**REMARKS**

Applicant appreciates the significant effort made by the Patent Office in the final Office Action to explain the basis for finding Applicant's prior rebuttal arguments unpersuasive. For example, the final Office Action includes a number of explanatory figures and accompanying analysis in the final Office Action, focused on Applicant's earlier rebuttal argument that Tanaka's NCO 9 does not generate an overall AFC/PLL circuit output signal. That amount of effort is unusual, and the Applicant greatly appreciates the Office's work in carefully explaining its rejection arguments.

However, Applicant notes several key problems readily apparent in the detailed rejection arguments presented by the Office as to why Tanaka (U.S. 5,909,148) allegedly anticipates independent claims 1, 10, and 24. For example, the final Office Action presents Fig. C as a PLL diagram that allegedly demonstrates why element 9 in Tanaka's drawings (NCO 9) can be argued as outputting a PLL clock signal within the meaning of Applicant's claims. In presenting this drawing, the Patent Office simply rearranges selected element blocks shown in Tanaka to make it appear that "NCO 9" provides a PLL circuit output signal. It is important to note that the Patent Office simply drew a signal "arrow" off of the internal feedback signal produced by NCO 9 to suggest that it goes somewhere other than to an internal feedback node in Tanaka's AFC/PLL circuit. **Further, Applicant notes that Fig. C presented by the Patent Office mislabels the output of NCO 9 as a frequency output signal "g(nT)," while the actual teachings of Tanaka show g(nT) as an input to NCO 9. Again, the output of NCO 9 serves as an internal feedback control signal that goes only to the PLL Complex Multiplying Device 8 of Tanaka's AFC/PLL circuit.**

It is equally telling that the Patent Office did not connect the NCO 9 output signal arrow to anything outside of Tanaka's AFC/PLL circuit. Indeed, the Patent Office could not in good faith offer such an illustration because it knows that NCO 9 of Tanaka produces only a feedback

signal that is purely internal to Tanaka's AFC/PLL circuit. Consequently, the NCO 9 signal cannot legitimately be argued as teaching Applicant's claimed PLL output clock signal. Applicant again notes that the "DEMODULATED SIGNAL," which the Patent Office does illustrate as going outside of Tanaka's AFC/PLL circuit, represents Tanaka's AFC/PLL circuit output signal, and it is not generated in the manner claimed by Applicant in independent claims 1, 10, and 24.

More particularly, consider Applicant's claim 1. Claim 1 in its entirety claims:

> A method of generating **an output clock signal from a phase-locked loop (PLL)**, the method comprising:
> determining **successive phase difference values between a reference clock signal and said output clock signal**;
> filtering said successive phase difference values to generate successive control values;
> **controlling a frequency of said output clock signal based on said successive control values**; and
> adapting a filter used to filter said successive phase difference values **based on average control values determined from said successive control values**.

(Emphasis added.)

Everything in claim 1 reinforces the point now repeatedly argued by Applicant. Namely, the methods and apparatus taught by Applicant relate to generating a PLL output signal that is provided to additional, downstream circuitry, and that is based on averaging control values determined from successive phase differences between the output signal and the input reference signal. With their consistent subject matter, the same characterizations apply to the remaining independent claims 10 and 24.

Against these claim details and careful explanations, the Patent Office erroneously argues that the internal feedback node element (NCO 9) in Tanaka produces a PLL output signal in accordance with Applicant's claims. This argument ignores the plain fact that Tanaka illustrates a DEMODULATED SIGNAL as its AFC/PLL output signal, and further plainly illustrates that NCO 9 does not produce a circuit output signal within the meaning of Applicant's claims. Indeed, the natural consequence of the Patent Office's reasoning is that literally any

circuit element anywhere within Tanaka's illustrated AFC/PLL circuit could be argued as producing a PLL output signal, without any regard for whether that signal was purely internal, and without any regard for that signal's use.

Moreover, Tanaka's NCO 9 does not produce its output signal in accordance with the claimed limitations regarding averaged control values. In more detail, claim 1 specifically claims determining successive phase differences between the reference clock signal input to a PLL circuit, and the output clock signal provided by the PLL circuit. Further, the claim stipulates that these successive phase differences are filtered to produce control values, and that the filter used to produce the control values is adapted based on the average of the control values. All of these details reinforce the relationship between the reference clock signal input to a PLL circuit, and the corresponding output clock signal output by the PLL circuit.

NCO 9 in Tanaka generates its feedback signal responsive to g(nT). At col. 4, line 66 – col. 5, line 26, Tanaka carefully explains that g(nT) is the output signal from a loop filter 11, and that the signal is proportional to the oscillation frequency of NCO 9. Moreover, Tanaka explains at col. 5, lines 43-50 that the "oscillating frequency of NCO 9 is controlled so that it becomes the residual frequency error of the AFC loop." Thus, by its plain language, Tanaka gives a definition to the output of NCO 9 that flatly contradicts the Patent Office's rejection arguments, and plainly demonstrates why it is legal error to argue that the output from NCO 9 is the same as Applicant's claimed PLL output clock signal.

Further, Tanaka does not teach filter adaptation within the meaning of claims 1, 10, and 24. For example, as noted, claim 1 stipulates that the filter used to generate control values for controlling the frequency of the claimed PLL output clock signal is adapted based on the average of those control values. In contrast, the loop filter 11 illustrated in Fig. 3 of Tanaka is updated based on setup data from memories 101 and 103, which corresponds to the output signal of Tanaka's data determining device 16. (See Tanaka at col. 6, lines 15-25.) As explained

at col. 4, lines 15-23, these memories store loop range and other parameters, such as frequency control width and control time intervals, for operating the AFC/PLL circuit of Tanaka.

As Applicant noted before, Tanaka is relevant in that it discloses an AFC/PLL circuit that is superficially similar to the circuits and methods detailed and claimed by Applicant. However, the fundamental circuit operations Applicant claims distinctly differ from the fundamental operations taught by Tanaka. The Patent Office's arguments and explanations are not consistent with the actual teachings of Tanaka, and they draw erroneous equivalence between carefully named and described signals and operations in Applicant's claims and unrelated, different signals and operations in Tanaka.

In the above arguments, Applicant fully drew out and explained the fundamental differences in between the claimed invention and Tanaka. Figs. A, B, and C presented by the Patent Office in the final Office Action provided a clear basis for highlighting the Patent Office's mischaracterizations of Tanaka, and for distinguishing Applicant's claims. Therefore, Applicant believes that independent claims 1, 10, and 24, and all their dependent claims, stand in condition for immediate allowance over Tanaka. Indeed, Applicant believes and hereby respectfully requests that all rejections based on Tanaka alone or in combination be withdrawn, and that all pending claims move forward to allowance.

Respectfully submitted,

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Dated: July 10, 2006

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